PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	Unknown
Filing Date	October 07, 2003
First Named Inventor	John K. Jennings
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	X-1339 US

OTHER -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/CN/		Lee, Thomas H. et al.; "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabytes/s DRAM"; IEEE Journal of Solid-State Circuits, Vol. 29, NO. 12, December 1994; pp. 1491-1496.	
/CN/		Maneatis, John G.; "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques"; IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; pp. 1723-1732.	
/CN/		Sidiropoulos, Stafanos; "A Semidigital Dual Delay-Locked Loop"; IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997; pp. 1683-1692.	
/CN/		Bult, Klaas et al.; "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm^2; IEEE Journal of Solid-State Circuits, Vol. 32, No. 12, December 1997; pp. 1887-1895.	
/CN/		Chou, Ju-Ming et al.; "A 125MHz 8b Digital-to-Phase Converter"; ISSCC 2003 / Session 24 / Clock Generation / Paper 24.8; two pages.	

Examiner Signature	/Chuong Ngo/	Date Considered	03/22/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.